Carrier-Based Modulation Strategies for Multimodular Matrix Converters

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***Abstract*—Based on the equivalency between the full-bridge indirect matrix converters (MCs) and the 3 × 1-modular MCs, the carrier-based modulation strategy is first tailored for the 3 3×1-modular MC. It can be directly expanded to $3\times N$-modular MC, but in order to improve the power quality, the phase-shifted (PS) method and phase disposition (PD) method are proposed. The former is suitable for the $3\times N$-modular MC with any multiwinding transformers (including phase-shifting transformers). Moreover, the latter is only applicable to the $3\times N$-modular MC with ordinary multiwinding transformers. The PD method has advantages over the PS method in the output current quality and efficiency. However, the PS method is superior to the PD method in the input current quality. Experimental results verify the correctness and effectiveness of the proposed modulation schemes.**

***Index Terms*—Carrier-based modulation, full-bridge indirect matrix converter (FIMC), multimodular matrix converter (MC), phase disposition (PD), phase shifted (PS).**

I. Introduction

THE matrix converter (MC) has attracted more and more attention due to the advantageous features such as sinusoidal input and output currents, bidirectional energy flow, controllable input displacement factor, and no need of dc-link capacitors [1]–[5]. However, the conventional MC is not suitable for medium-voltage or high-voltage applications due to the limited voltage ratings of the current power semiconductors. Combining the concept of multilevel converters [6] with MCs, lots of new topologies for multilevel MCs have emerged. In terms of topologies, the multilevel MC could mainly be divided into diode-clamped MCs [7]–[9], capacitor-clamped MCs [10]–[12], and multimodular MCs [13]–[17].

The multilevel diode-clamped MCs are developed based on the topology of the indirect MC (IMC). Generally, they consist of bidirectional current source rectifiers (CSRs) and diode-clamped inverters. A three-level MC is presented in [7], where a bidirectional CSR is cascaded to a three-level diode-clamped inverter, and the neutral point of the inverter is connected to the star point of the capacitors in the input filter. However, its input current quality degrades to some extent because the neutral point current is not taken into account. Reference [8] proposes a multilevel diode-clamped MC topology with reduced switches, and its input current quality is improved by keeping the average neutral point current zero. Multilevel output voltages are realized based on the aforementioned topologies, but the limited voltage rating of the power semiconductors makes them not suitable for medium-voltage applications. To overcome the aforementioned drawback, a new multilevel diode-clamped MC topology is proposed in [9], which includes multiple CSR modules connected in series and a matched multilevel diode-clamped inverter. The capacitor-clamped MC utilizes the delta-connected flying capacitors and additional bidirectional switches to provide more voltage levels, which improves the output current quality. However, the associated modulation strategy and control scheme are complicated [11]. In addition, the need of a larger number of capacitors makes it difficult to commercialize. The multimodular MC [13]–[17] inherits the idea of cascaded H-bridge (CHB) converters. It is formed by series connection of two or more three-phase input single-phase output MC cells (SPMC). Thus, one obvious advantage of the multimodular MC is its modularity and scalability to meet any output voltage level requirements. Compared with the conventional CHB converter whose basic cell is a three-phase active front-end rectifier-based power cell, the multimodular MC needs slightly more insulated gate bipolar transistors (IGBT) and diodes than that of the CHB converter [18]. However, a large number of bulky dc-link capacitors in the CHB converter are required to buffer the ripple energy of single-phase systems, which will increase the converter size and weight and decrease the converter lifetime greatly. Therefore, the multimodular MC has attracted much attention. Up to this point, it is the only multilevel MC product that has been commercialized and applied to skin-pass mill in steel process [17].

Lots of modulation strategies for the multimodular MC have been presented. A direct transfer function based modulation strategy is proposed in [14]. However, the voltage transfer ratio of the 3 × 1-modular MC (MMMC-I) is limited to 1.5. In [15], an indirect space vector modulation (SVM) which is based on the equivalency between 3 × 1-modular MCs and three-level indirect MCs is presented, and the voltage transfer ratio is expanded to 1.732. Moreover, the double line-to-line synthesis modulation for multimodular MCs is studied [16]. When the

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aforementioned modulation methods are expanded to $3 \times N$-modular MCs (MMMC-II), the idea of the phase-shifted (PS) pulsewidth modulation (PWM) is used.

As is well known, the SVM and carrier-based PWM are two commonly used methods in conventional two-level converters and multilevel converters. However, SVM becomes difficult to implement with the increase of the level number of the inverter, so the carrier-based modulation is preferred under this situation. In this paper, phase disposition (PD) and PS carrier-based modulations for multimodular MC are proposed. The underlying idea derives from the full-bridge IMC (FIMC). FIMC is a kind of three-level MC [19]. Usually, it is used to drive open-end winding induction motors without output transformers. The modulation strategy for FIMC is easy to design due to the similarity with IMC. In this paper, it is proved that the FIMC is a subset of the 3×1-modular MC. Therefore, any modulation scheme suited for FIMC could be transplanted to multimodular MCs conveniently.

The remainder of this paper is organized as follows. Section II introduces the relationship between the multimodular MC and FIMC. In Section III, the carrier-based modulation scheme for FIMC is presented. In Section IV, the corresponding modulation for the SPMC is introduced, and PD and PS carrier-based modulation methods for multimodular MC are deduced, followed by the input current calculations accordingly. In Section V, the experimental results are illustrated, and finally, the main points of this paper are summarized in Section VI.

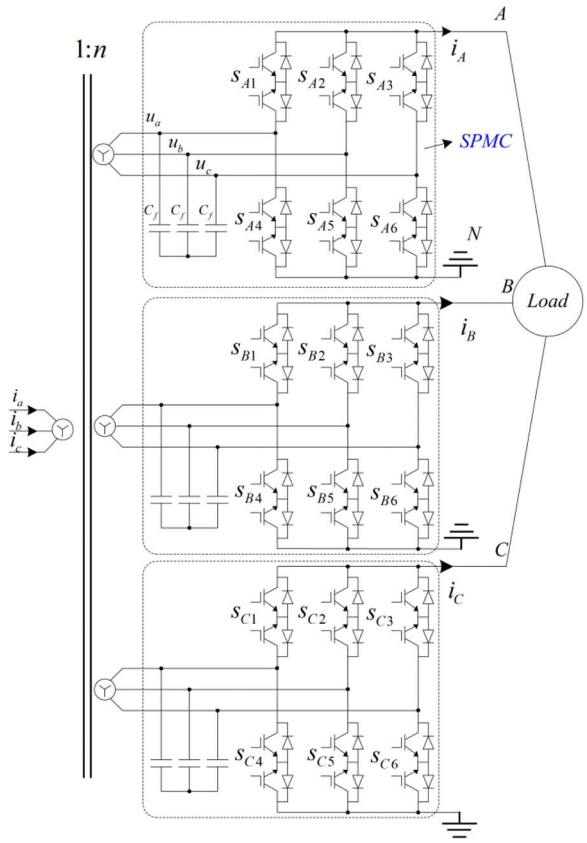


Fig. 1. Topology of a 3×1-modular MC.

II. Topological Structure

A. Topology of the Multimodular MC

A 3×1-modular MC topology structure is shown in Fig. 1. Its basic cell is an SPMC. Each SPMC consists of six bidirectional power switches, and each bidirectional power switch is realized by two IGBTs with antiparallel diode pairs connected to the common emitter. In the nomenclature of the 3×1-modular, "3" means that the converter has three phase outputs, and "1" means that each phase has only one SPMC. To gain a higher voltage and more levels of output voltages, multiple SPMC cells should be connected in series. For instance, a multimodular MC with N SPMC units connected in series in each phase is illustrated in Fig. 2. It is called as $3 \times N$-modular MCs.

B. Relationship Between 3×1-Modular MC and FIMC

The 3×1-modular MC is a three-level MC. The FIMC with isolated output transformers with the turns ratio of 1:1 in Fig. 3 is also a three-level IMC. According to Figs. 1 and 3, it is clear that the FIMC needs fewer power semiconductor switches than the 3×1-modular MC, which is an advantage in cost. The FIMC is mainly used to feed the induction/PM motors with open-end winding. To form multilevel MCs, isolated output transformers must be installed behind the FIMC. However, to avoid the excitation saturation of the isolated output transformers, the output voltage frequency of the multilevel MC made up of FIMC is very restricted in practice. Therefore, it lacks practicality.

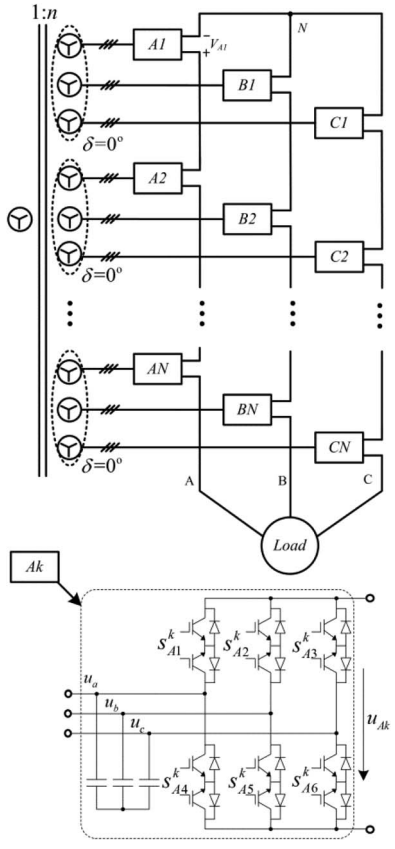


Fig. 2. Simplified diagram of a $3 \times N$-modular MC.

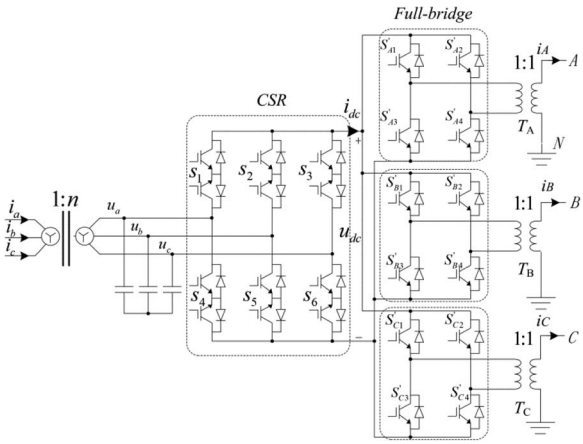


Fig. 3. Topology of the FIMC.

The purpose of the introduction of the FIMC is to help derive modulation schemes for the multimodular MC. As we all know, the research on multimodular MCs is rare compared to conventional MCs or IMCs. Recently, lots of modulation schemes have been proposed for the conventional MCs. However, it is not easy to apply the existing modulation methods to multimodular MCs directly. If we could prove the equivalency between the 3×1-modular MC and FIMC, modulation schemes suited for the FIMC could be transplanted to multimodular MCs based on the equivalency.

Regarding the 3×1-modular MC, according to Fig. 1, hence its output voltages and input currents can be written as follows:

$$u_{iN} = (S_{i1} - S_{i4})u_a + (S_{i2} - S_{i5})u_b + (S_{i3} - S_{i6})u_c \quad (1)$$

$$\begin{cases} i_a = n\left[\sum\limits_{i\in\{A,B,C\}} (S_{i1} - S_{i4})i_i + 3C_f \frac{du_a}{dt}\right] \\ i_b = n\left[\sum\limits_{i\in\{A,B,C\}} (S_{i2} - S_{i5})i_i + 3C_f \frac{du_b}{dt}\right] \\ i_c = n\left[\sum\limits_{i\in\{A,B,C\}} (S_{i3} - S_{i6})i_i + 3C_f \frac{du_c}{dt}\right] \end{cases} \quad (2)$$

where n represents the secondary-to-primary turns ratio of the transformer; u_a, u_b, and u_c are the secondary phase voltages of the transformer; S_{ij} denotes the state of a bidirectional switch (0—off, 1—on); and $i \in \{A, B, C\}$, $j \in \{1, 2, 3, 4, 5, 6\}$.

For the FIMC, according to Fig. 3, assume that the input side transformer turns ratio is the same as that in the 3×1-modular MC. Then, its output voltages and input currents are

$$u_{iN} = (S'_{i1} - S'_{i2})\left[(S_1 - S_4)u_a + (S_2 - S_5)u_b + (S_3 - S_6)u_c\right] \quad (3)$$

$$\begin{cases} i_a = n\left[(S_1 - S_4)\sum\limits_{i\in\{A,B,C\}} (S'_{i1} - S'_{i2})\, i_i + 3C_f \frac{du_a}{dt}\right] \\ i_b = n\left[(S_2 - S_5)\sum\limits_{i\in\{A,B,C\}} (S'_{i1} - S'_{i2})\, i_i + 3C_f \frac{du_b}{dt}\right] \\ i_c = n\left[(S_3 - S_6)\sum\limits_{i\in\{A,B,C\}} (S'_{i1} - S'_{i2})\, i_i + 3C_f \frac{du_c}{dt}\right] \end{cases} \quad (4)$$

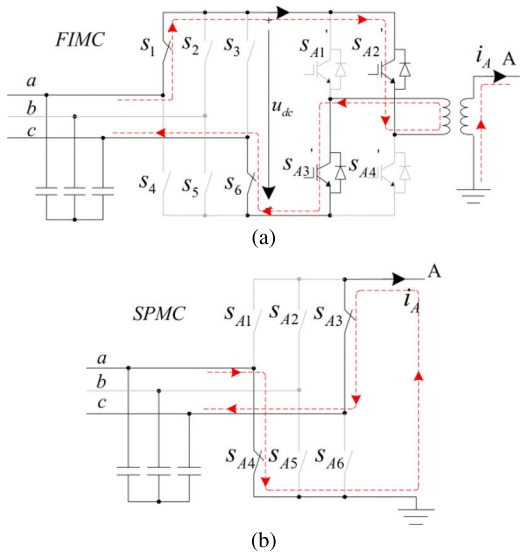


Fig. 4. Operating conditions for a given switching state. (a) FIMC. (b) 3×1-modular MC.

where $S_1 \sim S_6$ denote the state of the switch in the rectifier and S'_{i1} and S'_{i2} denote the switch states in the H-bridge inverters, $i \in \{A, B, C\}$.

If the following equations have feasible solutions at any time, the two types of MCs mentioned previously are equivalent in terms of input currents and output voltages

$$\begin{cases} S_{i1} - S_{i4} = (S_1 - S_4)(S'_{i1} - S'_{i2}) \\ S_{i2} - S_{i5} = (S_2 - S_5)(S'_{i1} - S'_{i2}) \\ S_{i3} - S_{i6} = (S_3 - S_6)(S'_{i1} - S'_{i2}) \end{cases} \quad (5)$$

$$\begin{cases} S_{i1} + S_{i2} + S_{i3} = 1 \\ S_{i4} + S_{i5} + S_{i6} = 1. \end{cases} \quad (6)$$

It can be verified that, for any given feasible switching state combination in Fig. 3, there exists at least one switching state combination in Fig. 1 satisfying (5) and (6). Taking the output phase-A for example, Fig. 4(a) shows an operating condition of the FIMC for a given feasible switching state. Its equivalent switching state in the 3×1-modular MC is shown in Fig. 4(b). Clearly, the switching states in Fig. 4 satisfy (5) and (6) simultaneously.

However, on the contrary, it is not always possible that there exists a corresponding switching state in Fig. 3 being equivalent to the given switching state in Fig. 1. For example, a 3×1-modular MC could output three different voltages at an instant, while the FIMC cannot. Therefore, it can be concluded that the topology 3×1-modular MC contains the topology FIMC in functionality. In practice, because the switching states in the aforementioned example are rarely used, not too strictly, the 3×1-modular MC is regarded as equivalency to the FIMC.

III. Modulation Scheme for FIMC

The modulation strategies for IMC have been well studied [20]–[24], which include SVM, carrier-based modulation, and other modulations. The IMC and FIMC are similar in topology; the distinction is that the inverter in IMC is a half-bridge

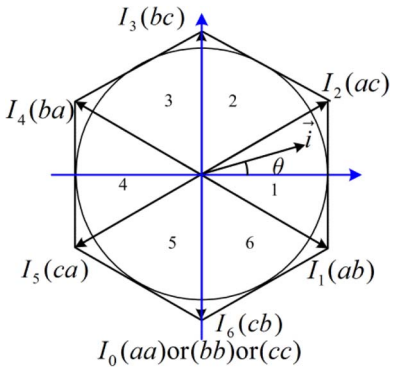


Fig. 5. Space vector diagram for the rectifier modulation.

converter while it is a full-bridge inverter in FIMC. Therefore, an SVM modulation for the FIMC could be obtained by combining the methods in [4] and [25]. Although the SVM is more flexible in implementation, the complexity increases quickly when the level number of the inverter gets higher. In this paper, the carrier-based modulation (i.e., min-max-SPWM) for the FIMC will be introduced in detail. The reason is twofold. First, the FIMC has a physical dc-link, which makes it suitable for the carrier-based modulation. Second, it is natural to apply the existing multicarrier-based PWM schemes to the multilevel MC being made up of the FIMC.

A. SVM for Rectifier

The current space vector diagram for the rectifier modulation is shown in Fig. 5. As shown, there are six sectors $1 \sim 6$, six active vectors $I_1 \sim I_6$, and three zero vectors $I_7 \sim I_9$. In each sector, the adjacent active vectors and zero vectors can be used to synthesize the desired input current vector $\vec{i}$, where each vector corresponds to a switching state of the rectifier.

Based on the current space vector synthesis principle, the duty ratios of the adjacent active vectors and zero vectors can be expressed as follows:

$$\begin{cases} d_1 = \sin\left(\pi/6 - [\theta - (m-1)\pi/3]\right) \\ d_2 = \sin\left(\pi/6 + [\theta - (m-1)\pi/3]\right) \\ d_0 = 1 - d_1 - d_2 \end{cases} \tag{7}$$

where d_1, d_2, and d_0 are the duty ratios of the active and zero vectors, respectively. θ represents the angular position of the current vector, and m $(m = 1, 2, \ldots, 6)$ denotes the current vector sector.

Assuming that the input voltage vector referred to the transformer secondary side is denoted as $\vec{u} = U_{im}e^{j\theta_c}$, then $\theta = \theta_c + \phi$, where U_{im} and θ_c are the amplitude and phase angle of the input voltage vector, respectively, and ϕ is the power factor angle.

In order to reduce the commutation times and maximize the voltage utilization, zero vectors are not used here, which can also make the following carrier-based modulation easy to implement. Therefore, the corresponding duty ratios are normalized as follows:

$$\begin{cases} d_\alpha = \frac{d_1}{(d_1+d_2)} = k(\theta)\sin\left(\pi/6 - [\theta - (m-1)\pi/3]\right) \\ d_\beta = \frac{d_2}{(d_1+d_2)} = k(\theta)\sin\left(\pi/6 + [\theta - (m-1)\pi/3]\right) \end{cases} \tag{8}$$

where $k(\theta) = 1/\cos[\theta - (m-1)\pi/3]$.

The average dc-link voltage during each switching period can be calculated as

$$\overline{u}_{dc} = \frac{3}{2}k(\theta)\cdot\cos\phi\cdot U_{im}. \tag{9}$$

From (9), it can be found that the dc-link voltage fluctuates with six times the input frequency.

B. Carrier-Based Modulation for the Inverter

The carrier-based modulation for IMC is introduced in [22]–[24]. It mainly consists of two procedures: modulated signal calculation and PWM signal generation.

Assume that the desired output phase voltages are

$$\begin{cases} u_{AN} = U_{om}\cos(\omega_o t) \\ u_{BN} = U_{om}\cos(\omega_o t - 2\pi/3) \\ u_{CN} = U_{om}\cos(\omega_o t + 2\pi/3) \end{cases} \tag{10}$$

where U_{om} and ω_o are the amplitude and angular frequency of the output voltages, respectively.

The modulation signals can be written as

$$\begin{cases} u_{AO} = u_{AN} + u_{NO} \\ u_{BO} = u_{BN} + u_{NO} \\ u_{CO} = u_{CN} + u_{NO} \end{cases} \tag{11}$$

where u_{AO}, u_{BO}, and u_{CO} are the modulated signals, and u_{NO} denotes the zero-sequence signal. Usually, to maximize the utilization of the dc-link voltage, the zero-sequence signal u_{NO} is chosen by

$$u_{NO} = -\frac{\min(u_{AN}, u_{BN}, u_{CN}) + \max(u_{AN}, u_{BN}, u_{CN})}{2}. \tag{12}$$

For the convenience of analysis and implementation, the modulated signals u_{AO}, u_{BO}, and u_{CO} are normalized as

$$\overline{u}_{iO} = \frac{u_{iO}}{\overline{u}_{dc}}, \quad i \in \{A, B, C\}. \tag{13}$$

Moreover, they satisfy the following constraints

$$-1 \le \overline{u}_{iO} \le 1. \tag{14}$$

Assuming that the input current vector is located in sector 1, according to Fig. 5, the modulation process for the rectifier is shown in Fig. 6(a). The resulting dc-link voltage is made up of two line-to-line voltages: $u_{\rm ab}$ and $u_{\rm ac}$.

As for the modulation process of inverters, for simplicity, only the phase-A H-bridge inverter is taken for example to illustrate the modulation process. In multicarrier-based PWM schemes, generally, the PD and phase opposition disposition methods are commonly used. To improve the output current quality of the FIMC, the PD method is applied as shown in Fig. 6(b) and (c). Two triangle carrier signals (carrier1 and carrier2) with the same phase are used. The binary PWM outputs for switches S'_{A1} and S'_{A3} are produced by comparing carrier1 with the modulated signal $\overline{u}_{AO}$, and the binary PWM

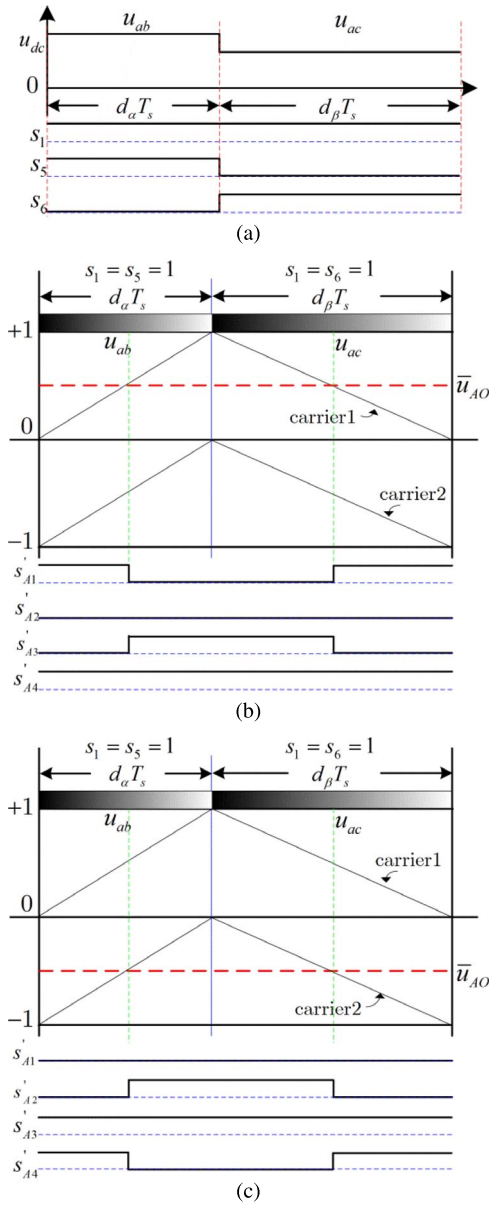


Fig. 6. Schematic diagrams and related switching patterns. (a) Rectifier stage. (b) Inverter stage under $\overline{u}_{AO} \geq 0$. (c) Inverter stage under $\overline{u}_{AO} < 0$.

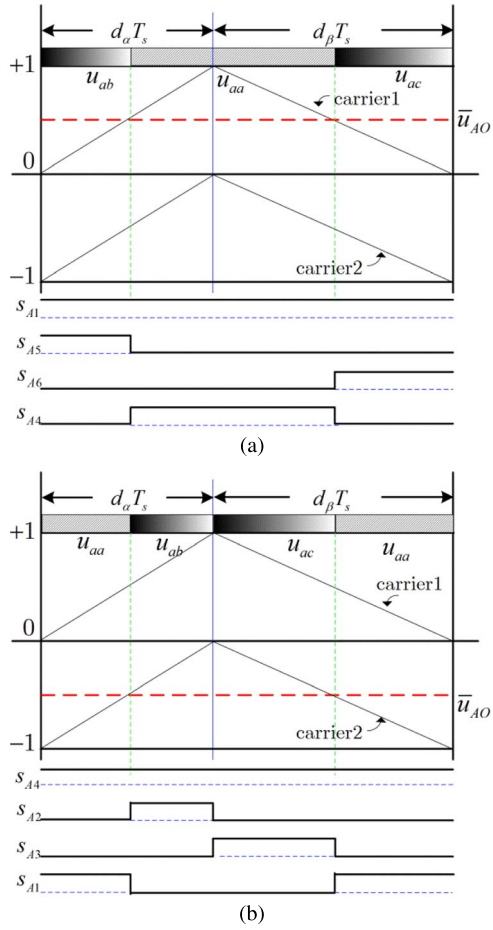


Fig. 7. Corresponding switching patterns of the SPMC. (a) $\overline{u}_{AO} \geq 0$. (b) $\overline{u}_{AO} < 0$.

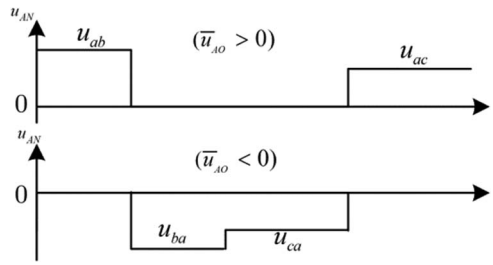


Fig. 8. Output phase voltage waveform.

outputs for switches S'_{A4} and S'_{A2} are produced by comparing carrier2 with the modulated signal $\overline{u}_{AO}$.

IV. Modulation Scheme for Multimodular MC

A. Modulation for SPMC

By analogy with the modulation of FIMC mentioned in the previous section, the modulation process for the phase-A SPMC is presented in Fig. 7. Fig. 7(a) shows the switching state when the modulated signal is greater than zero. In this case, S_{A1} is on, S_{A2} and S_{A3} are off in a modulation period, and the other three switches on the lower side conduct alternately (one and only switch in the upper or lower switches of an SPMC conducts at any time). Fig. 7(b) shows the case when the modulated signal is less than zero. In accordance with the modulation shown in Fig. 7, the corresponding output voltages are illustrated in Fig. 8.

In order to improve the input/output power quality, a double-sided symmetry switching pattern is adopted. The modulation schematic diagram under $\overline{u}_{AO} < 0$ is presented in Fig. 9. The switching sequences for SPMC-A1 are illustrated in Table I, for example, where "$S_{A1} - S_{A2}$" means that S_{A1} turns off and S_{A2} turns on. The other SPMCs also obey to the switching sequence similar to that in phase-A SPMC.

B. PS Carrier-Based Modulation for Multimodular MC

A $3 \times N$-modular MC is formed with N units of 3×1-modular MC in series. Thus, the constraint for modulation signals in (14) is changed as

$$-N \leq \overline{u}_{iO} \leq N. \tag{15}$$

TABLE I
SWITCHING SEQUENCE WITH THE DOUBLE-SIDED SYMMETRY PD METHOD

Current vector sector m	Polarity of $\overline{u}_{Ao}$	Switching sequence	Device (ON)
1	+	S_{A5}-S_{A4}-S_{A6}-S_{A4}-S_{A5}	S_{A1}
	-	S_{A1}-S_{A2}-S_{A3}-S_{A1}-S_{A3}-S_{A2}-S_{A1}	S_{A4}
2	+	S_{A1}-S_{A3}-S_{A2}-S_{A3}-S_{A1}	S_{A6}
	-	S_{A6}-S_{A4}-S_{A5}-S_{A6}-S_{A5}-S_{A4}-S_{A6}	S_{A3}
3	+	S_{A6}-S_{A5}-S_{A4}-S_{A5}-S_{A6}	S_{A2}
	-	S_{A2}-S_{A3}-S_{A1}-S_{A2}-S_{A1}-S_{A3}-S_{A2}	S_{A5}
4	+	S_{A2}-S_{A1}-S_{A3}-S_{A1}-S_{A2}	S_{A4}
	-	S_{A4}-S_{A5}-S_{A6}-S_{A4}-S_{A6}-S_{A5}-S_{A4}	S_{A1}
5	+	S_{A4}-S_{A6}-S_{A5}-S_{A6}-S_{A4}	S_{A3}
	-	S_{A3}-S_{A1}-S_{A2}-S_{A3}-S_{A2}-S_{A1}-S_{A3}	S_{A6}
6	+	S_{A3}-S_{A2}-S_{A1}-S_{A2}-S_{A3}	S_{A5}
	-	S_{A5}-S_{A6}-S_{A4}-S_{A5}-S_{A4}-S_{A6}-S_{A5}	S_{A2}

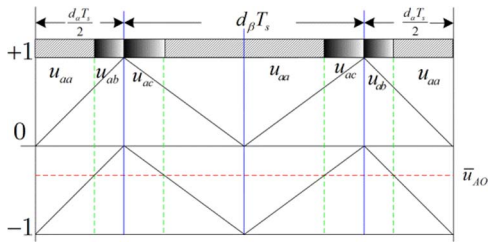


Fig. 9. Double-sided symmetry switching pattern of the SPMC under the PD method.

In theory, if each 3×1-modular MC works in the completely same way with the modulated signal as (16), the goal of generating the required output voltages could be achieved easily

$$\overline{u}_{i1} = \overline{u}_{i2} = \cdots = \overline{u}_{ik} = \frac{\overline{u}_{io}}{N}, \quad 1 \le k \le N \tag{16}$$

where $\overline{u}_{Ak}$, $\overline{u}_{Bk}$, and $\overline{u}_{Ck}$ denote the modulation signals for SPMC A_k, B_k, and C_k, respectively.

However, by this way, large voltage change rates (dv/dt) will occur in the output voltages, which induces the damaging circulating currents and corona discharge between the winding layers [26]. In addition, the output current quality is not satisfactory. To overcome the aforementioned drawbacks, the PS carrier-based modulation is a simple solution, which shifts the phase of each carrier by $2\pi/N$. The schematic diagram of the PS method is shown in Fig. 10; carrier 1 and carrier $1'$ are used to modulate SPMC A_1, B_1, and C_1; carrier 2 and carrier $2'$ are used to modulate SPMC A_2, B_2, and C_2; and carrier N and carrier N' are used to modulate SPMC A_N, B_N, and C_N. It is worth noting that the carriers in Fig. 10 are only used to explain the carrier phase characteristic; for details, please refer to Fig. 9.

C. PD Carrier-Based Modulation for Multimodular MC

The isolated transformer of the multimodular MC could be a multiwinding phase-shifting transformer [14]–[17] or an ordinary multiwinding transformer without phase-shifting. In fact, compared to the former transformer, the latter has an advantage in cost. In addition, the PD carrier-based modulation as shown in Fig. 11 is suited for the case when the multiwinding transformer without phase-shifting is used.

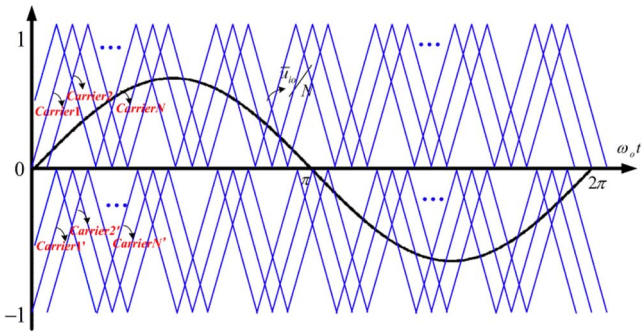


Fig. 10. Schematic diagram under the PS method for the multimodular MC.

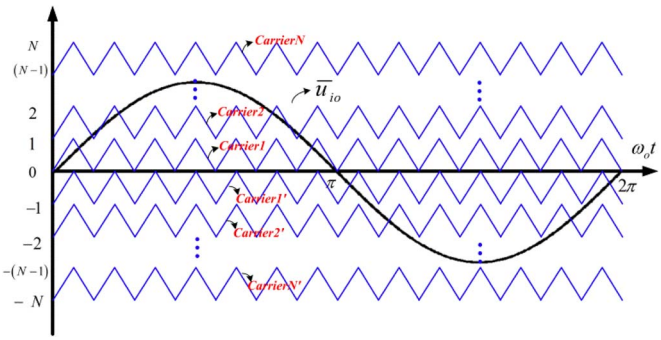


Fig. 11. Schematic diagram under the PD method for the multimodular MC.

According to Fig. 11, the modulation signal of each SPMC unit can be expressed as

$$\overline{u}_{ik} = \begin{cases} \text{sign}(\overline{u}_{io}), & k < X \\ [|\overline{u}_{io}| - (X-1)]\,\text{sign}(\overline{u}_{io}), & k = X \\ 0, & k > X \end{cases} \tag{17}$$

where $X = \text{ceil}(|\overline{u}_{io}|)$, the ceil functions map a real number to the smallest following integer.

D. Loss Comparison Between the PS and PD Methods

Before carrying out power loss comparisons, assume that the multimodular MC operates at the same carrier frequency under the PD and PS methods.

Usually, the power losses of the semiconductor devices include conduction losses and switching losses, which are related to the topology structure and the modulation strategy. The conduction losses of the multimodular MC under the PS and PD methods are completely the same because there are always two IGBTs and two diodes conducting at any instant in each SPMC. Therefore, only the calculations of the switching losses for both methods are necessary for the power loss comparisons.

The switching losses are generally assumed proportional to the switching voltage and the conducting current in a switching

period [27]. Thus, the turn-on loss, turn-off loss, and diode reverse recovery loss are represented as follows:

$$\begin{cases} E_{\text{on}} = k_{\text{on}} u_s i_s \\ E_{\text{off}} = k_{\text{off}} u_s i_s \\ E_{rr} = k_{rr} u_s i_s \end{cases} \tag{18}$$

where the coefficients k_{on}, k_{off}, and k_{rr} can be obtained from datasheets or experiments, and u_s and i_s are the voltage across the switch in OFF-state and the current through the switch in ON-state.

Without loss of generality, still assume the current vector located in sector 1. As shown in Fig. 8 and Table I, there is one turn-on, turn-off, and reverse recovery switching loss for an SPMC with modulation signal $|\overline{u}_{Ao}| = 1$. The SPMC with modulation signal $|\overline{u}_{Ao}| = 0$ does not have switching loss. While the modulation signal satisfies $-1 < \overline{u}_{Ao} < 0$ and $0 < \overline{u}_{Ao} < 1$, there are three times and two times turn-on, turn-off, and reverse recovery switching losses in total, respectively.

Hence, the total switching losses in an SPMC under different modulated signals in a modulation period can be derived as

$$E_i = \begin{cases} k_s u_{bc}|i_i|, & \overline{u}_{ik} = -1 \\ k_s(u_{ab} + u_{bc} + u_{ac})|i_i|, & -1 < \overline{u}_{ik} < 0 \\ 0, & \overline{u}_{ik} = 0 \\ k_s(u_{ab} + u_{bc})|i_i|, & 0 < \overline{u}_{ik} < 1 \\ k_s u_{bc}|i_i|, & \overline{u}_{ik} = 1 \end{cases} \tag{19}$$

where $k_s = k_{\text{on}} + k_{\text{off}} + k_{rr}$. From (19), it can be found that the switching losses under the condition $-1 < \overline{u}_{ik} < 0$ and $0 < \overline{u}_{ik} < 1$ are higher than those in the other conditions like $\overline{u}_{ik} = 1, -1$, and 0. According to (16) and (17), it can be seen that the modulated signals of each SPMC under the PS method satisfy the condition $-1 < \overline{u}_{ik} < 0$ or $0 < \overline{u}_{ik} < 1$. However, under the PD method, only three SPMCs in the $3 \times N$-modular MC meet the condition: $-1 < \overline{u}_{ik} < 0$ or $0 < \overline{u}_{ik} < 1$. Moreover, the other SPMC cells suffer from less switching losses. Thus, it is clear that the total switching losses under the PS method are larger than those in the PD method. However, according to the aforementioned analysis, it can be concluded that each SPMC has different switching losses under the PD method. Therefore, to distribute the switching losses uniformly, the modulated signal in each SPMC should be exchanged.

E. Input Current Derivations

Assume that the leakage inductance at the secondary side of the isolated transformer is negligible, the three-phase load is linear and balanced, and the desired output phase voltages are sinusoidal and balanced.

According to Fig. 2, the input currents at the transformer primary side could be expressed as

$$\begin{cases} i_a = n \sum_{k=1}^{N} i_{ak} \\ i_b = n \sum_{k=1}^{N} i_{bk} \\ i_c = n \sum_{k=1}^{N} i_{ck}. \end{cases} \tag{20}$$

For simplicity, only the a-phase input current is considered first. In (20), i_{ak} is the a-phase current of the kth secondary winding. Without loss of generality, assume that the desired input current vector lies in sector 1. From (2), i_{ak} can be given as

$$i_{ak} = \sum_{i \in \{A,B,C\}} \left(d_{i1}^k - d_{i4}^k\right) i_i + 3C_f \frac{du_a}{dt} \tag{21}$$

where d_{i1}^k, d_{i4}^k $(i \in \{A, B, C\})$ represent the duty ratios of the switches S_{i1}^k, S_{i4}^k in the SPMC A_k, B_k, and C_k, respectively; $3C_f(du_a/dt)$ is the current through the filter capacitors.

According to Fig. 7, d_{i1}^k, d_{i4}^k can be expressed as

$$d_{i1}^k = \begin{cases} \overline{u}_{ik}, & \text{when } \overline{u}_{io} \geq 0 \\ 0, & \text{when } \overline{u}_{io} < 0 \end{cases} \tag{22}$$

$$d_{i4}^k = \begin{cases} 0, & \text{when } \overline{u}_{io} \geq 0 \\ -\overline{u}_{ik}, & \text{when } \overline{u}_{io} < 0. \end{cases} \tag{23}$$

Substituting (22) and (23) into (21), i_{ak} can be expressed as

$$i_{ak} = \sum_{i \in \{A,B,C\}} \overline{u}_{ik} i_i + 3C_f \frac{du_a}{dt}. \tag{24}$$

Then, after some manipulations with (9)$\sim$(13), (20), and (24), i_a can be written as

$$\begin{aligned} i_a &= n\left(i_A \sum_{k=1}^{N} \overline{u}_{Ak} + i_B \sum_{k=1}^{N} \overline{u}_{Bk} + i_C \sum_{k=1}^{N} \overline{u}_{Ck} + 3NC_f \frac{du_a}{dt}\right) \\ &= n\left(\overline{u}_{AO} i_A + \overline{u}_{BO} i_B + \overline{u}_{CO} i_C + 3NC_f \frac{du_a}{dt}\right). \end{aligned} \tag{25}$$

In steady state, i_a can be formulated as

$$i_a = I\cos(\theta_c + \phi) - I_C \sin(\theta_c) \tag{26}$$

where $I_C = 3nNC_f\omega U_{im}$, $I = 2nP_o/3U_{im}$, $P_o = u_A i_A + u_B i_B + u_C i_C$, and it represents the output active power of the MC.

Equation (26) can be further simplified as

$$i_a = I_s \cdot \sin(\theta_c + \varphi) \tag{27}$$

where $I_s = \sqrt{I^2 + I_c^2 + 2I \cdot I_C \sin\phi}$ and $\varphi = \arctan(-I\cos\phi/(I\sin\phi + I_C))$.

Similarly, the b- and c-phase input currents (i_b and i_c) could also be obtained as follows:

$$i_b = -nd_\alpha(\overline{u}_{Ao} i_A + \overline{u}_{Bo} i_B + \overline{u}_{Co} i_C) = I_s \cos(\theta_c + \varphi - 2\pi/3) \tag{28}$$

$$i_c = -nd_\beta(\overline{u}_{Ao} i_A + \overline{u}_{Bo} i_B + \overline{u}_{Co} i_C) = I_s \cos(\theta_c + \varphi + 2\pi/3). \tag{29}$$

From the aforementioned derivations, it is clear that one necessary condition to guarantee sinusoidal input currents is

$$\sum_{k=1}^{N} \overline{u}_{ik} = \overline{u}_{io}, \quad i \in \{A, B, C\}. \tag{30}$$

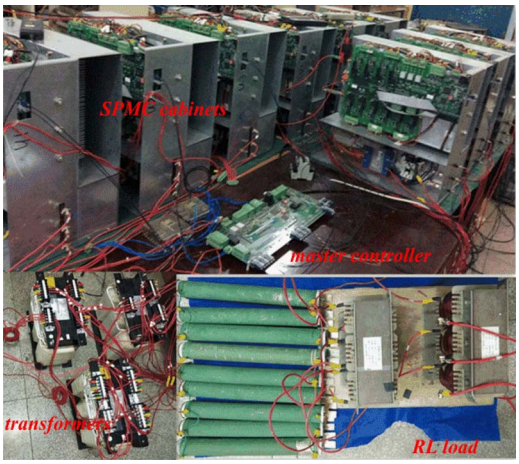


Fig. 12. Experimental setup for the 3 × 3-modular MC.

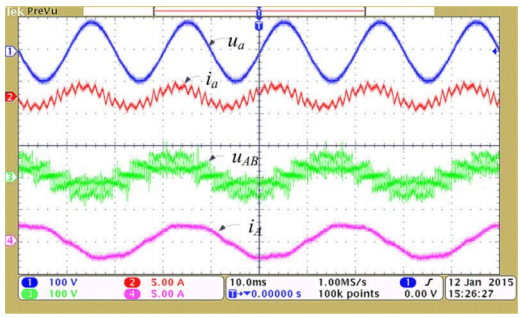
TABLE II
PARAMETERS USED IN THE EXPERIMENTS

Parameters	Value
Input line-to-line voltage (U_i)	0.158 p. u.
Grid frequency	50 Hz
Input filter capacitor (C)	0.52 p. u.
Load resistor (R)	8.3 Ω
Load inductance (L_o)	6 mH
Sampling frequency (f_s)	2 kHz
Transformer ratio	380V/100V (Yy0)
Nominal power of transformer	10 KVA
Leakage inductance	0.01 p. u.

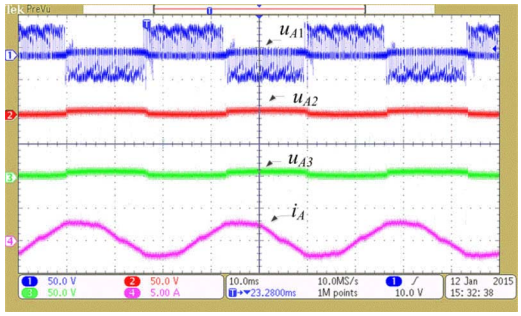
Moreover, it is nothing to do with the arrangement of the modulation signal for each SPMC. Therefore, both PS method and PD method are feasible modulation strategy for the multimodular MC.

V. EXPERIMENTAL RESULTS

To validate the proposed modulation methods, an experimental setup for the 3 × 3-modular MC shown in Fig. 12 has been developed in the laboratory. The related parameters are listed in Table II. The carrier frequency is equal to the sampling frequency. The 3 × 3-modular MC prototype includes the following: a three-phase ordinary multiwinding transformer, one master control board, nine SPMC control cabinets, and a three-phase balanced RL load. Each SPMC control cabinet is composed of a slave controller board, a main circuit of the SPMC, IGBT driver boards, and a clamp circuit. A master–slave control scheme is adopted in this work. The master control board communicates with the slave controller boards via optical fibers. The master controller board is mainly composed of a floating-point DSP (TMS320F28335) and a field-programmable gate array (EP2C8J144C8N), which is responsible for the related calculation and signal transmission.



(a)



(b)

Fig. 13. Experimental results under the PD method ($q = 1.5$, and $f_o = 30$ Hz).

The slave controllers have almost the same hardware configuration with the main controller board. It is responsible for receiving the signals from the master controller and generating the PWM signals for the IGBTs. In addition, the slave controller needs to monitor the status of each SPMC cabinet and transmit the fault signal to the master controller.

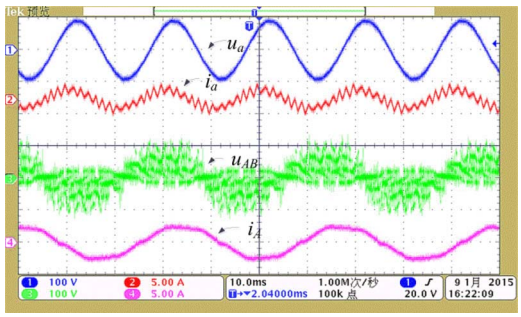
To commute the current in a safe way, the current-based four-step commutation method is applied for each SPMC.

For convenience, the voltage transfer ratio is defined as $q = U_{om}/U_{im}$. The experiments are carried out in the following cases:

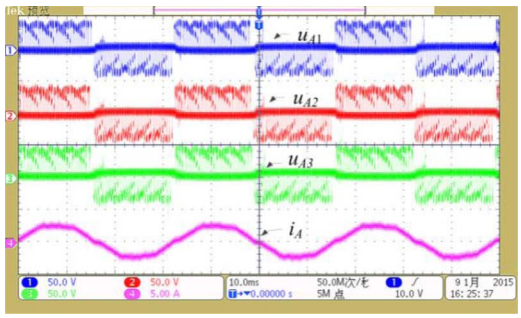
1) $q = 1.5$, $f_o = 30$ Hz;
2) $q = 4.5$, $f_o = 30$ Hz;
3) $q = 5.2$, $f_o = 60$ Hz;

where f_o is the frequency of the output voltages.

In case I, the experimental waveforms under the PD method and PS method are shown in Figs. 13 and 14, respectively. In Figs. 13(a) and 14(a), from top to bottom, they are the input voltage u_a, input current i_a, output line-to-line voltage $u_{\rm AB}$, and output current i_A, respectively. As shown, the input and output currents in both PD method and PS method are almost the same and sinusoidal. However, the profiles of the output line-to-line voltages are different. In Figs. 13(b) and 14(b), u_{A1}, u_{A2}, and u_{A3} are the output voltages of SPMC A_1, A_2, and A_3, respectively. Since the voltage transfer ratio is less than 1.73 in this case, the modulation signals of two SPMC cells are always equal to zero in the PD method. That is to say, the two output voltages of the SPMC cells must be zero, which could be verified by Fig. 13(b). It is worth noting that u_{A2} and u_{A3} are not equal to zero in fact, which is due to the voltage drop of the semiconductor devices. As shown in Fig. 14(b), the waveforms

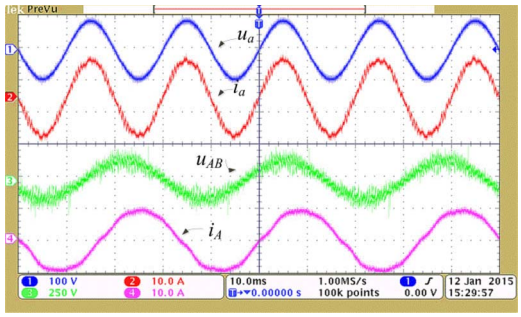


(a)

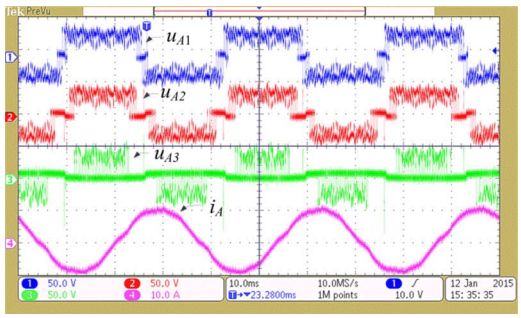


(b)

Fig. 14. Experimental results under the PS method ($q = 1.5$, and $f_o = 30$ Hz).



(a)

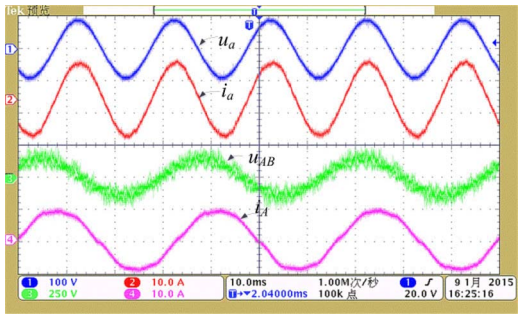


(b)

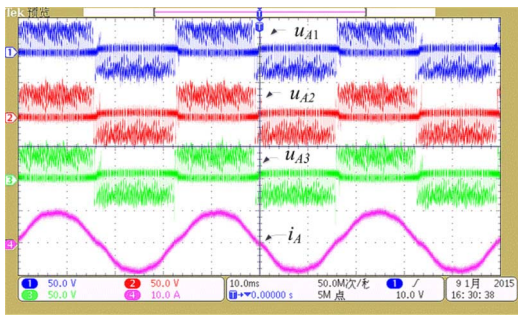
Fig. 15. Experimental results under the PD method ($q = 4.5$, and $f_o = 30$ Hz).

of u_{A1}, u_{A2}, and u_{A3} are almost identical, except for a small phase displacement caused by the PS carriers, which coincides with the theoretical analysis before.

In case II, the associated experimental results with the PD method and PS method are shown in Figs. 15 and 16, respectively. It is obvious that the 3×3-modular MC operates at unity input power factor under the two aforementioned modulation



(a)



(b)

Fig. 16. Experimental results with the PS method ($q = 4.5$, and $f_o = 30$ Hz).

methods. Meanwhile, it is clear that the input current ripple under the PS method is less than that under the PD method. With the voltage transfer ratio increasing, more voltage levels are used to synthesize the output voltages in the PD method. Thus, its output line-to-line voltage shown in Fig. 15(a) is more close to an ideal sinusoidal waveform than in Fig. 16(a). From Fig. 15(b), it can be found that the output voltages of SPMC A_1, A_2, A_3 are different from each other under the PD method. Moreover, according to the waveforms of u_{A1} and u_{A2}, it can be found that u_{A1} and u_{A2} are made up of two nonzero line-to-line voltages for a long time. Fig. 16(b) shows that the output voltage waveforms of SPMC A_1, A_2, A_3 under the PS method are basically consistent, which is the same as that in case I. Thus, based on the waveforms of the SPMC cells, we could infer that the switching loss under the PD method is less than that under the PS method.

In case III, the voltage transfer ratio is increased to 5.2, which is close to the theoretically maximum value. Moreover, the frequency of the output voltages is changed from 30 to 60 Hz. The related experimental results are shown in Fig. 17. As shown, there are no significant changes in the experimental waveforms, except for the output frequency.

To evaluate the power quality of the input and output currents quantitatively under the PD and PS methods, the Fourier analysis is carried out. The measured total harmonic distortion (THD) values for the input currents and output currents under different q values are shown in Fig. 18. It can be concluded that the PD method is superior to the PS method in output current quality. On the contrary, the PS method can obtain better input current quality than the PD method. In addition, it can be found that both input current quality and output current quality become better with increasing output voltages.

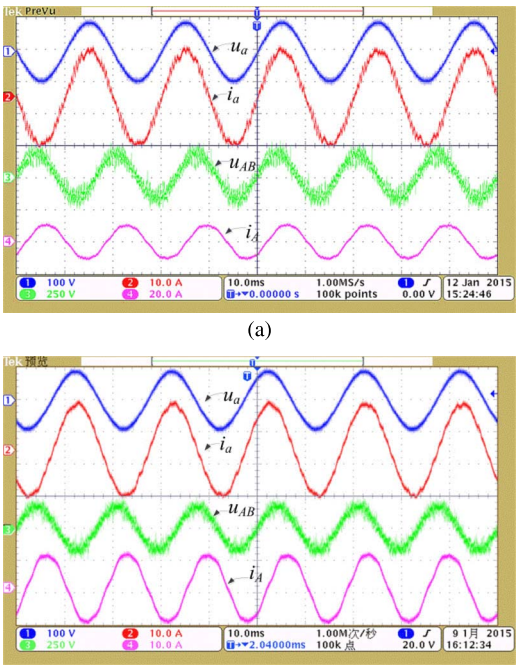


Fig. 17. Experimental results under $q = 5.2$ and $f_o = 60$ Hz. (a) PD method. (b) PS method.

In these experiments, all of the input currents in the tests do not meet IEEE 519-1992 limits. The possible reasons for the degraded input and output current quality mainly include the dead-time involved in the four-step commutation strategy, the voltage drop due to IGBTs and diodes, the poorly designed input filters, and the no-load currents in the transformer. According to the scheme diagram of the 3×3-modular MC, it can be found that up to six IGBTs and six diodes are connected in series in each output loop at any instant. In the case of low transfer ratios, the voltage deviation due to the voltage drop covers a relatively large proportion in output voltages. As a result, the corresponding THD value of the output currents is large. Because the input currents and the output currents have direct coupling relations as shown in (2), the input currents will also suffer from distortion accordingly. With the increase of voltage transfer ratios, the voltage deviation due to the voltage drop covers a relatively smaller proportion, so the resulting THD value of the output currents becomes smaller, which coincides with the experimental results. There are two classes of solutions to improve the input current quality. One is to minimize or eliminate the nonlinearity sources. The nonlinear compensation methods proposed in [28]–[30] can be used for references. The other is to design input filters [31] with good performance. In multimodular MC, the leakage inductances of the three-phase ordinary multiwinding transformer serve as the input filter inductances. Thus, the design of the transformer is critical. In addition, a proper damping of the input filter is needed to stabilize the system and to attain high-quality input currents.

VI. Conclusion

To reduce the cost of the multimodular MC, a multiwinding phase-shifting transformer is replaced by an ordinary multi-

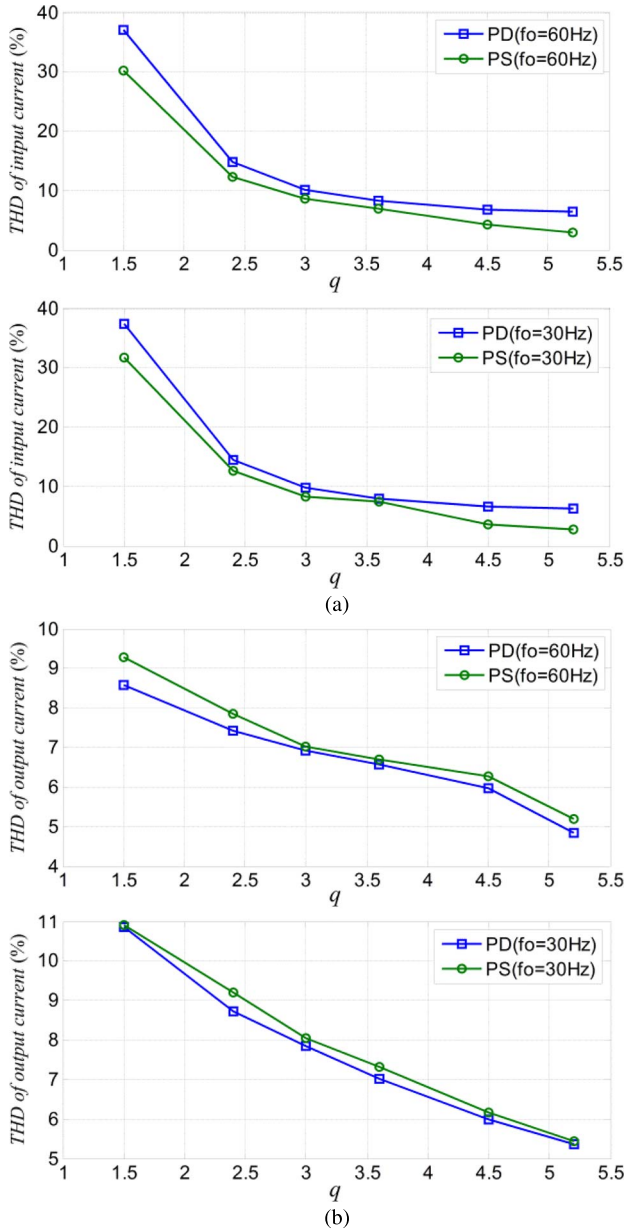


Fig. 18. Measured THD of the input currents and output currents for the 3×3-modular prototype. (a) THD of the input currents. (b) THD of the output currents.

winding transformer. Based on the multimodular MC, two carrier-based modulation methods have been proposed, which are derived from the similarity with FIMCs. It is proved that the input currents of the multimodular MC are sinusoidal under the proposed modulation methods when feeding a three-phase balanced linear load.

Compared to other existing modulations, it is convenient for the carrier-based modulation methods to be expanded to multilevel cases. In the proposed methods, the PD method has an advantage over the PS method in output current quality and efficiency. However, it is not easy to distribute the power loss of each semiconductor device uniformly. The PS method has an advantage over the PD method in input current quality. Meanwhile, the loss distribution of each SPMC under the PS

method is uniform. Intuitively, it is possible to combine the PS and PD methods to improve the comprehensive performance in input and output currents, which is worth studying in the future.

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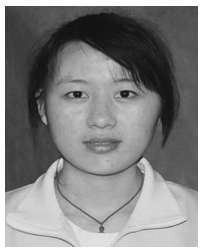

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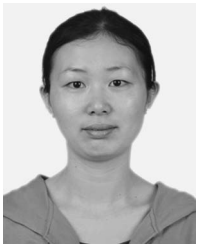

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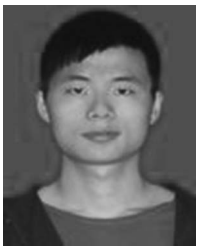

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